PATENT ABSTRACTS OF JAPAN

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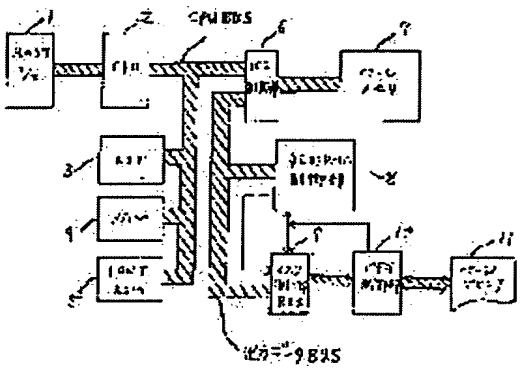
SONOMURA NAGAMASA
BABA ICHIRO

(54) IMAGE RECTANGULAR DMA SYSTEM

(57)Abstract:
PURPOSE: To reduce a burden on a CPU and enhance a total throughput by a method wherein rectangular image data on an arbitrary position of a page memory is transmitted to a printer in a DMA system.
CONSTITUTION: A CPU 2 sets an address of an arbitrary rectangular area on a page memory in a rectangular DMA control part 8 in a bit expression. In the rectangular control part 8, an address and an effective bit are found by a start point and an end point in an X direction. Only data stored in the rectangular area is accessed.



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CLAIMS

[Claim(s)]
[Claim 1]Picture rectangle DMA system which can carry out the DMA output of the image data created on a page memory by giving arbitrary rectangle parameters in a page printer represented by laser beam printer to a page memory which this page printer has directly at a page printer.
[Claim 2]The picture rectangle DMA system according to claim 1 which expresses a pause of said arbitrary data of a rectangle parameter with bitwise instead of a byte unit, and carries out the DMA transfer of the rectangle data in a fine unit.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention can prevent the intervention of a processor (henceforth CPU) as much as possible in a page printer with a page memory, It is related with the DMA system which performs DMA (Direct Memory Access) transmission and enabled it to output fine rectangle data on a page printer by giving arbitrary rectangle parameters for the image data on a page memory.
[0002]
[Description of the Prior Art]The output from the page memory to the conventional page printer, CPU is divided roughly into the method which performs data transfer to the buffer for direct page printers per byte using the method which performs the DMA transfer of an one-line unit via an exclusive DMA controller, or FIFO (first in, first out).
[0003]
[Problem(s) to be Solved by the Invention]However. [whether in the conventional method, when outputting image data to a page printer from a page memory, CPU sets a parameter as an exclusive DMA controller for every line, and] Or the fall of the total throughput was carried out for the method that CPU writes immediate data in printer buffers, such as FIFO. The load of CPU was increasing to the clipping processing of the dot unit for processing in which it writes in on a dummy-spaces memory. This invention is what improved the method to which a printer is made to carry out the DMA transfer of the rectangle data, the fall of a total throughput is prevented and there is a place made into the purpose in reducing the load of CPU.
[0004]
[Means for Solving the Problem]That is, there is a means for attaining the purpose in considering it as DMA system with a rectangle control section which controls only a memory of a tip value of a rectangle given by bitwise of a page memory of a printer, and a termination value.
[0005]
[Function]The tip value of the rectangle to which the image data by which the operation was created on the page memory was given by bitwise from CPU (x_1, y_1), The required bit of parameter x_1 and x_2 is included for the image data which needs a rectangle control section than a termination value (x_2, y_2) from a memory address tip value (x_1, y_1) per byte to a termination value (x_2, y_2), It is possible to transmit without the intervention of CPU from a page memory to the video processing section to a plotter via a system bath at the time of transmission.
[0006]
[Example]Hereafter, one example of this invention is explained in full detail based on a drawing. Drawing 1 is an entire configuration figure for explaining the picture rectangle DMA system of this invention, FONTROM which 1 made the host computer and 2 made CPU and to which, as for ROM and 4, three carried out the memory of the letter symbol for release of drawing, as for RAM and 5, In [as for rectangle direct memory access control and 9, a bus controlling part and 7 are / a video control section and 11 / page printers a mask control register and 10 a page memory and 8 6, and] drawing 1, If the image data outputted by HOST1 to ROM3, RAAM4, and

FONTROM5 is inputted into the page memory 7 by CPU2 via the bus controlling part 6 and the image data for one sheet is completed, The conditions outputted to the page printer 11 are set as the rectangle direct memory access control 8, according to the video requirement signal from the video control section 10, the rectangle direct memory access control 8 begins operation, and required [to a change / via the ** bus controlling part 6 and the mask control register 9] for the page printer 11 in a CPU bus and an output data bus -- image data transfer is carried out.

[0007]Next, by giving the arbitrary rectangle parameters made into the gist of this invention explains the method which carries out the DMA output of the picture created on the page memory 7 directly at the page printer 11 based on drawing 1, referring to drawing 2 (a), (b), (c), drawing 3, and drawing 4. In [drawing 2 (a), (b), and (c) is an explanatory view showing the example of the page memory 7, and] a figure (a), The image data for one sheet outputted by CPU2 is shown, and The peak value of the page memory 7 (0, 0), What is necessary is to transmit only this shadow area 7a to the page printer 11, if it is a termination value (x_e, y_e), a tip value (x_1, y_1) of the rectangle which gave the slash, and a termination value (x_2, y_2). Usually, although it is **** to which this shadow area 7a is transmitted by the page printer 11 by CPU per byte, In this invention, moreover, it transmits to the page printer 11 by bitwise, and this transmission is not based on CPU, but by instructions of the video control section 10, the rectangle direct memory access control 8 begins to operate, and the shadow area 7a is transmitted to the page printer 11.

[0008]The explanation transmitted by this bitwise is explained based on a figure (b) and (c). A figure (b) shows the invalidity to 1 byte of a tip value (x_1, y_1) (it is henceforth called a tip address), and the number of effective bits, and a figure (c) shows the invalidity to 1Byte of a termination value (x_2, y_2) (it is henceforth called an end address), and the number of effective bits. Usually, the validity in 1 byte since a DMA transfer is 1 byte, 2 bytes, or 4 bytes and 1 byte is 8 bits and the number of invalid bits, When an invalid bit is set to alpha, when = $(x_1/8)$ n_1- (alpha/8) and the number of effective bits are set to beta, drawing 2 (c) is shown by = $(x_2/8)$ n_2- (beta/8) in drawing 2 (b). Here, n_1 shows the tip address in arbitrary values, and the end address in values with arbitrary n_2.

[0009]On the upper page memory, these addresses are actually expressed with tip address (x_e+1) y_1+n_1 and end address (x_e+1) y_2+n_2. However, in the case of alpha!=0 and beta!=0, about a x direction, the number of effective bits of the address of x_1 and x_2 is set to beta respectively (8-alpha). In the case of beta= 0, it is set to end address (x_e+1) y_2+n_2-1. When a MASK byte expresses here the invalid bit of 0-7 bits of data which comprises 1 byte (8 bits) with a binary system, Since all binary systems can be expressed by a low rank (side which went to 0 bit directions from 7-bit side when x_e direction address of drawing 1 is 0, 1, and 2.....7 bits is shown) triplet, a triplet is needed. Thus, although it is a translation in which a DMA transfer is carried out to the page printer 11 by operation of the rectangle direct memory access control 8 by fine bitwise, a logic circuit explains the operation below.

[0010]Drawing 3 is a block diagram of the rectangle direct memory access control of x, and The tip address of the rectangular shadow area 7a (x_1, y_1), A set of an end address (x_2, y_2) and end address x_e of the page memory 7 will change DMA into Byte with each dividers 12 and 16 first for Byte transmission. About low rank 3 Bit of low rank 3 Bit $(x_2/8)$ of each MASK Bit $(x_1/8)$, as drawing 1 explained, it is used for processing of the number of effective bits. However, in order to process the above-mentioned termination Adlai ** (x_e+1) y_2+n_2-1 with the subtractor 18 in the case of low rank 3 Bit=0 of $(x_2/8)$, the value of $x_2/(8)-1$ is set to the comparator 19. And if GOF/F which is a seizing signal is set to this control section from CPU and XCLK which is an image synchronizing signal is inputted from the video control section 10, The counter 14 moves and it is searched [of a x direction] whether a counter value is larger [by the comparator 13]

in effective value than (x_1/8), or equal. If the value of the x counter 14 becomes equal to x_e, the Y counter 20 will be counted up one time. The effective value of the direction of Y also becomes effective by whether a counter value is larger than y_1 or equal by the comparator 21. And the terminal point of a x direction is detected by the comparator 19. The terminal point of Y_2 is similarly detected by the Y_2 comparator 22.

[0011]The shadow area 7a which is the effective value of drawing 1 as mentioned above is detected. In order that the value of x counter and Y counter may become Lower and a Upper address respectively in the address to the page memory 7 or a memory read signal may not come only out of the above-mentioned useful range in the memory read control part 23, the total throughput of CPU improves also at this point. Drawing 4 is a block diagram which determines the starting point of the x direction shown by drawing 1, and the effective bits of an end part, and, in the case of the starting point, a low rank triplet, In order to change into 8 bits, it is inputted into the mask 24 in the timing of x and MSKSET, and it is reversed (effective-bits 8-alpha), and an output is set in the register 30 by the 8-bit register 30 in the timing of an iolite signal (I/OW) through the gate of the gate circuit 25. When X_1MSKSET is an imitation, it is set in the register 30 through the gate circuit 26 (when it is not the starting point of a x direction). In the case of the terminal point of a x direction, a low rank (x_2/8) triplet is changed into 8 bits through the mask 27 in the timing of X_2 MSK, and an output remains as it is and is set in the register 30 through the gate circuit (effective-bits beta) 28. When X_2MSKSET is an imitation (it is not a terminal point of a x direction), it is set in the register 30 through the gate circuit 25.

[0012]

[Effect of the Invention]As explained above, according to this invention, the DMA transfer of the data created without the intervention of CPU on the page memory from the page memory for page printers can be carried out to a page printer at high speed, And in order to access the data of only a required rectangle portion on a page memory, a total throughput becomes large extremely. Since a pause of the data of arbitrary rectangle parameters is not a byte unit but bitwise and clipping of a dot unit of it becomes possible in hard, it can decrease the load of a total throughput and CPU.

[0013]

[Translation done.]

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TECHNICAL FIELD

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PRIOR ART

[Description of the Prior Art]The output from the page memory to the conventional page printer, CPU is divided roughly into the method which performs data transfer to the buffer for direct page printers per byte using the method which performs the DMA transfer of an one-line unit via an exclusive DMA controller, or FIFO (first in, first out).

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EFFECT OF THE INVENTION

[Effect of the Invention]As explained above, according to this invention, the DMA transfer of the data created without the intervention of CPU on the page memory from the page memory for page printers can be carried out to a page printer at high speed, And in order to access the data of only a required rectangle portion on a page memory, a total throughput becomes large extremely. Since a pause of the data of arbitrary rectangle parameters is not a byte unit but bitwise and clipping of a dot unit of it becomes possible in hard, it can decrease the load of a total throughput and CPU.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]However. [whether in the conventional method, when outputting image data to a page printer from a page memory, CPU sets a parameter as an exclusive DMA controller for every line, and] Or the fall of the total throughput was carried out for the method that CPU writes immediate data in printer buffers, such as FIFO. The load of CPU was increasing to the clipping processing of the dot unit for processing in which it writes in on a dummy-spaces memory. This invention is what improved the method to which a printer is made to carry out the DMA transfer of the rectangle data, the fall of a total throughput is prevented and there is a place made into the purpose in reducing the load of CPU.

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MEANS

[Means for Solving the Problem]That is, there is a means for attaining the purpose in considering it as DMA system with a rectangle control section which controls only a memory of a tip value of a rectangle given by bitwise of a page memory of a printer, and a termination value.

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OPERATION

[Function]The tip value of the rectangle to which the image data by which the operation was created on the page memory was given by bitwise from CPU (x_1, y_1), The required bit of parameter x_1 and x_2 is included for the image data which needs a rectangle control section than a termination value (x_2, y_2) from a memory address tip value (x_1, y_1) per byte to a termination value (x_2, y_2), It is possible to transmit without the intervention of CPU from a page memory to the video processing section to a plotter via a system bath at the time of transmission.

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EXAMPLE

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[0007]Next, by giving the arbitrary rectangle parameters made into the gist of this invention explains the method which carries out the DMA output of the picture created on the page memory 7 directly at the page printer 11 based on drawing 1, referring to drawing 2 (a), (b), (c), drawing 3, and drawing 4. In [drawing 2 (a), (b), and (c) is an explanatory view showing the example of the page memory 7, and] a figure (a), The image data for one sheet outputted by CPU2 is shown, and The peak value of the page memory 7 (0, 0), What is necessary is to transmit only this shadow area 7a to the page printer 11, if it is a termination value (x_e, y_e), a tip value (x_1, y_1) of the rectangle which gave the slash, and a termination value (x_2, y_2). Usually, although it is **** to which this shadow area 7a is transmitted by the page printer 11 by CPU per byte, In this invention, moreover, it transmits to the page printer 11 by bitwise, and this transmission is not based on CPU, but by instructions of the video control section 10, the rectangle direct memory access control 8 begins to operate, and the shadow area 7a is transmitted to the page printer 11.
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[0009]On the upper page memory, these addresses are actually expressed with tip address (x_e+1) y_1+n_1 and end address (x_e+1) y_2+n_2. However, in the case of alpha!=0 and beta!=0, about a x direction, the number of effective bits of the address of x_1 and x_2 is set to beta respectively

(8-alpha). In the case of beta= 0, it is set to end address (x_e+1) y_2+n_2-1. When a MASK byte expresses here the invalid bit of 0-7 bits of data which comprises 1 byte (8 bits) with a binary system, Since all binary systems can be expressed by a low rank (side which went to 0 bit directions from 7-bit side when x_e direction address of drawing 1 is 0, 1, and 2.....7 bits is shown) triplet, a triplet is needed. Thus, although it is a translation in which a DMA transfer is carried out to the page printer 11 by operation of the rectangle direct memory access control 8 by fine bitwise, a logic circuit explains the operation below.

[0010]Drawing 3 is a block diagram of the rectangle direct memory access control of x, and The tip address of the rectangular shadow area 7a (x_1, y_1), A set of an end address (x_2, y_2) and end address x_e of the page memory 7 will change DMA into Byte with each dividers 12 and 16 first for Byte transmission. About low rank 3 Bit of low rank 3 Bit (x_2/8) of each MASK Bit (x_1/8), as drawing 1 explained, it is used for processing of the number of effective bits. However, in order to process the above-mentioned termination Adlai ** (x_e+1) y_2+n_2-1 with the subtractor 18 in the case of low rank 3 Bit=0 of (x_2/8), the value of x_2/(8)-1 is set to the comparator 19. And if GOF/F which is a seizing signal is set to this control section from CPU and XCLK which is an image synchronizing signal is inputted from the video control section 10, The counter 14 moves and it is searched [of a x direction] whether a counter value is larger [by the comparator 13] in effective value than (x_1/8), or equal. If the value of the x counter 14 becomes equal to x_e, the Y counter 20 will be counted up one time. The effective value of the direction of Y also becomes effective by whether a counter value is larger than y_1 or equal by the comparator 21. And the terminal point of a x direction is detected by the comparator 19. The terminal point of Y_2 is similarly detected by the Y_2 comparator 22.

[0011]The shadow area 7a which is the effective value of drawing 1 as mentioned above is detected. In order that the value of x counter and Y counter may become Lower and a Upper address respectively in the address to the page memory 7 or a memory read signal may not come only out of the above-mentioned useful range in the memory read control part 23, the total throughput of CPU improves also at this point. Drawing 4 is a block diagram which determines the starting point of the x direction shown by drawing 1, and the effective bits of an end part, and, in the case of the starting point, a low rank triplet, In order to change into 8 bits, it is inputted into the mask 24 in the timing of x and MSKSET, and it is reversed (effective-bits 8-alpha), and an output is set in the register 30 by the 8-bit register 30 in the timing of an iolite signal (I/OW) through the gate of the gate circuit 25. When X_1MSKSET is an imitation, it is set in the register 30 through the gate circuit 26 (when it is not the starting point of a x direction). In the case of the terminal point of a x direction, a low rank (x_2/8) triplet is changed into 8 bits through the mask 27 in the timing of X_2 MSK, and an output remains as it is and is set in the register 30 through the gate circuit (effective-bits beta) 28. When X_2MSKSET is an imitation (it is not a terminal point of a x direction), it is set in the register 30 through the gate circuit 25.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]Drawing 1 is an imaged figure of a page memory where effective image data is stored.

[Drawing 2]Drawing 2 (a), (b), and (c) is a block diagram showing the composition of the picture rectangle DMA transfer method of this example.
[Drawing 3]Drawing 3 is a block diagram which performs the rectangle DMA control and the page memory address generation in an example.
[Drawing 4]Drawing 4 is a block diagram which determines the effective bits of the starting point of the x direction on the page memory in an example, and a terminal point.
[0014]
[Description of Notations]
1 Host computer
2 CPU
3 ROM
4 RAM
5 FONTROM
6 Bus controlling part
7 Page memory
8 Rectangle direct memory access control
9 Mask control register
10 Video control section
11 Page printer

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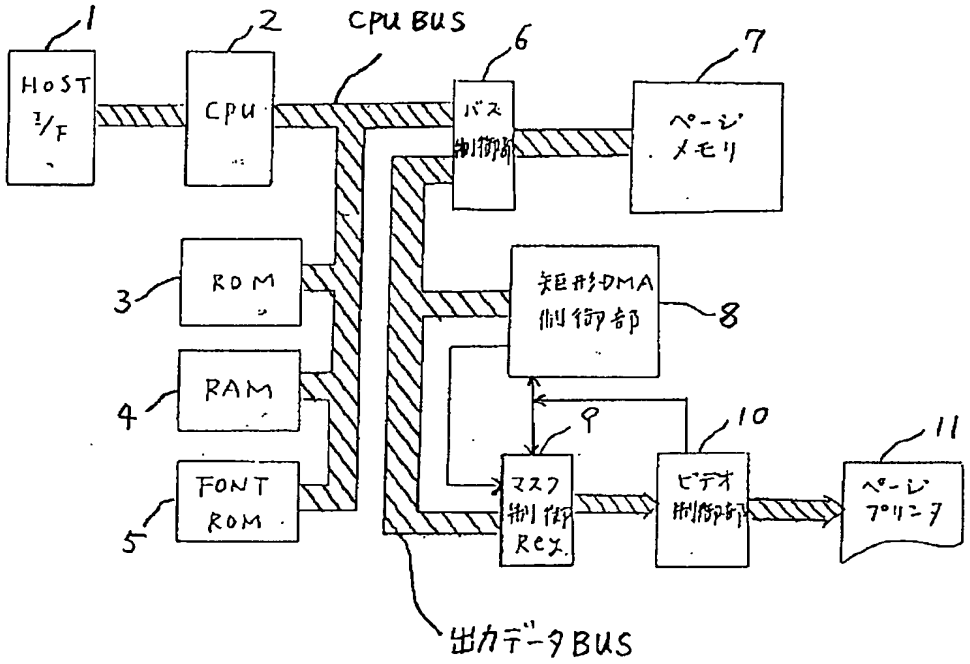
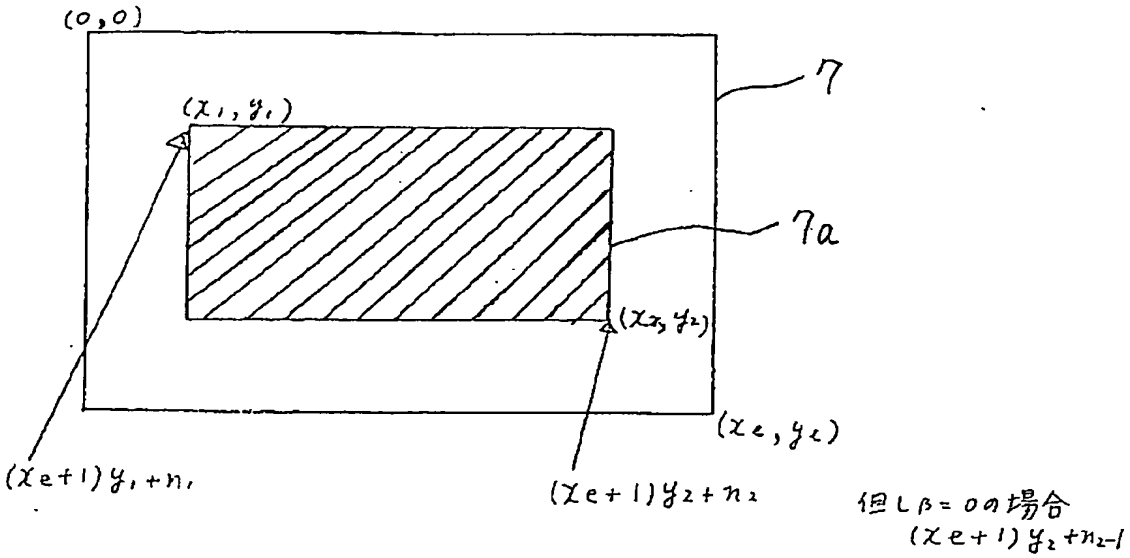
DRAWINGS

[Drawing 1]



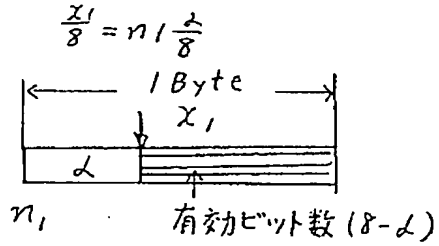
[Drawing 2]

(a)

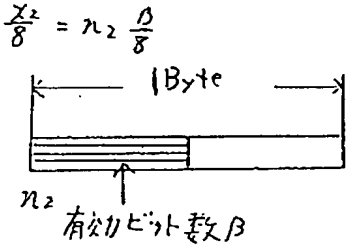


但しβ=0の場合
(xe+1) y2 + n2-1

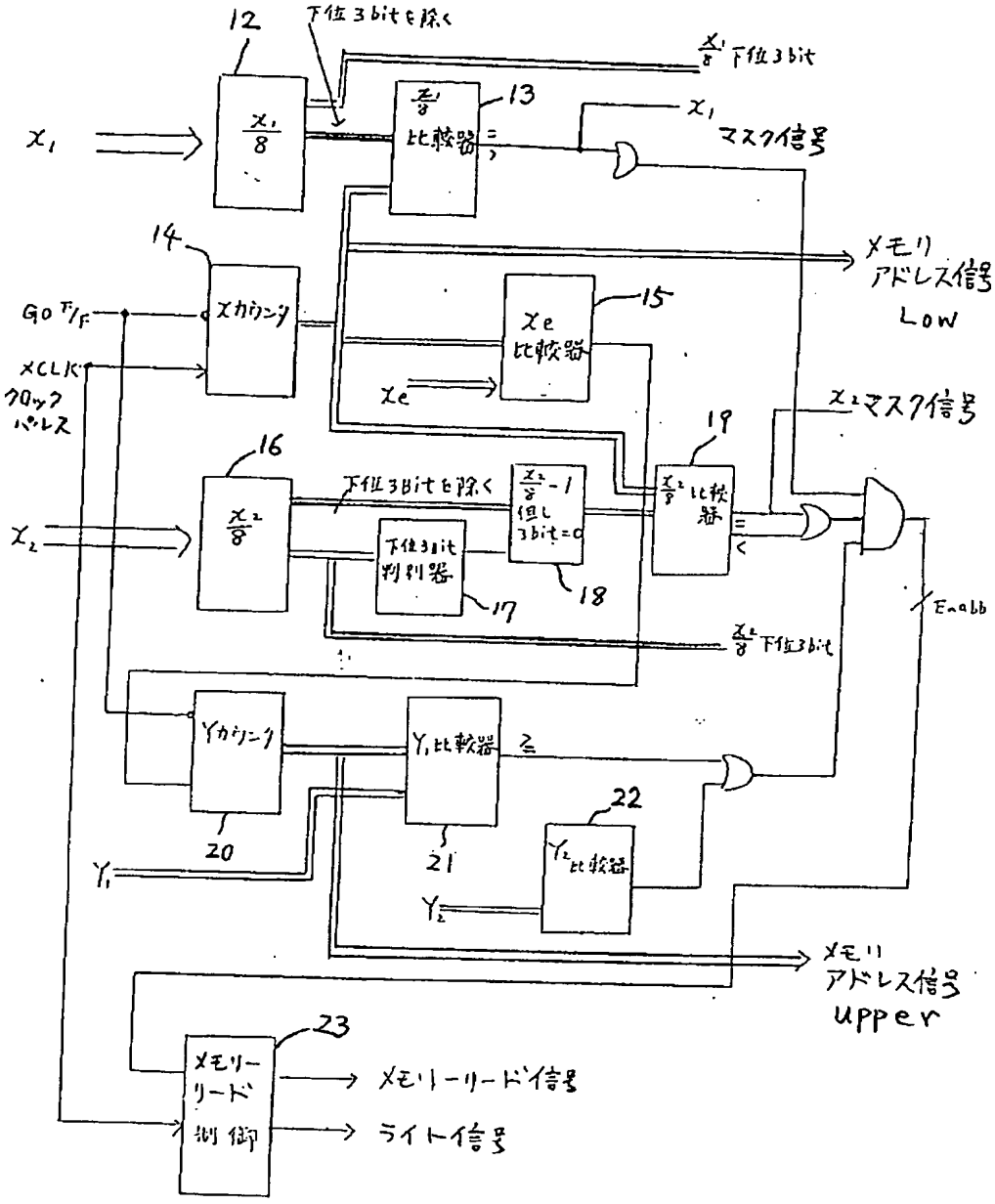
(b)



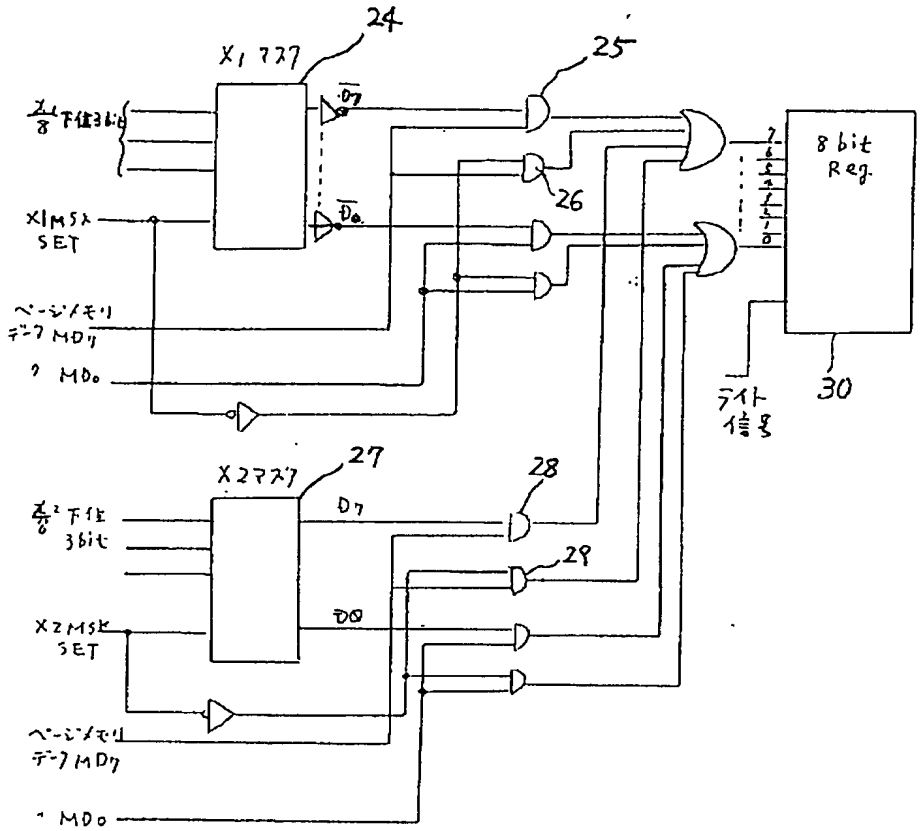
(C)



[Drawing 3]


12
下位3bitを除く
X1/8下位3bit
X1
13
X1/8 比較器
X1 マスク信号
14
メモリ アドレス信号 Low
GO F/F
Xカウンタ
XCLK
クロック パルス
Xe 比較器
15
Xe
X2マスク信号
19
16
X2/8
下位3bitを除く
X2/8 - 1 但し 3bit=0
X2/8 比較器
下位3bit判別器
17
18
X2
Enable
X2/8下位3bit
Yカウンタ
Y1比較器
Z
22
20
21
Y1
Y2
Y2比較器
メモリ アドレス信号 upper
23
メモリーリード制御
メモリーリード信号
ライト信号

[Drawing 4]



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(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号

特開平5－193203

(43)公開日　平成５年(1993)８月３日

(51)Int.Cl.[6]		識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｂ４１Ｊ	5/30		Ｚ　8907－2Ｃ		
	29/38		Ｚ　8804－2Ｃ		
Ｇ０６Ｆ	15/64	４５０	Ｅ　8840－5Ｌ		
Ｈ０４Ｎ	1/387		4226－5Ｃ		

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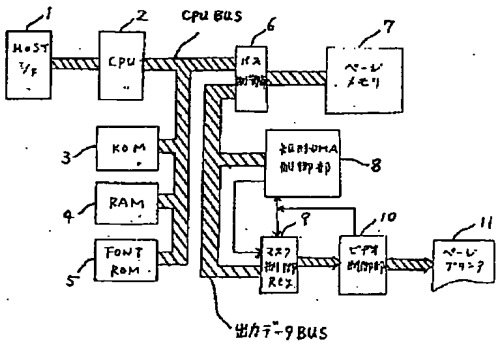
(54)【発明の名称】　画像矩形ＤＭＡ方式

(57)【要約】

【目的】ページメモリ上の任意の位置の矩形画像データをプリンタにＤＭ転送することにより、ＣＰＵの負担を減らし、トータルスループットを向上させることにある。

【構成】ＣＰＵはビット表現でページメモリ上の任意の矩形領域のアドレスを矩形ＤＭＡ制御部に設定し、この矩形ＤＭＡ制御部でＸ方向の始点，終点からアドレス及び有効ビットを求め、矩形領域のメモリだけをアクセスする方式である。



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【特許請求の範囲】

【請求項1】　レーザプリンタに代表されるページプリンタにおいて、このページプリンタがもっているページメモリに対し、任意の矩形パラメータを与える事によってページメモリ上に作成された画像データを直接ページプリンタにDMA出力できる画像矩形DMA方式。

【請求項2】　前記任意の矩形パラメータのデータの区切りを、バイト単位でなくビット単位で表わし、きめ細かい単位で矩形データをDMA転送する請求項1記載の画像矩形DMA方式。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、ページメモリを持つページプリンタに於て、プロセッサ（以下CPUという）の介在を出来るだけ防げ、ページメモリ上の画像データを、任意の矩形パラメータを与える事によりページプリンタ上にきめ細かい矩形データをDMA（ダイレクトメモリアクセス）転送を行い、出力できるようにしたDMA方式に関する。

【0002】

【従来の技術】従来のページプリンタへのページメモリからの出力は、専用DMAコントローラを介して1ライン単位のDMA転送を行なう方式か、あるいはFIFO（ファーストイン、ファーストアウト）等を用いてCPUが直接ページプリンタ用バッファに1バイト単位にデータ転送を行なう方式に大別されている。

【0003】

【発明が解決しようとする課題】しかしながら、従来の方式においては、ページメモリからページプリンタに画像データを出力する際にCPUが専用DMAコントローラに1ライン毎にパラメータを設定するか、又はFIFO等プリンタバッファにCPUが直接データを書き込むという方式の為、トータルスループットの低下をさせていた。又、ドット単位のクリッピング処理にダミースペースメモリ上に書き込むという処理の為、CPUの負荷が増大していた。本発明は矩形データをプリンタにDMA転送させる方式を改良したもので、その目的とするところは、トータルスループットの低下を防ぐと共に、CPUの負荷を軽減することにある。

【0004】

【課題を解決するための手段】つまり、その目的を達成するための手段は、プリンタのページメモリのビット単位で与えられた矩形の先端値、終端値のメモリのみを制御する矩形制御部をもったDMA方式とすることにある。

【0005】

【作用】その作用は、ページメモリ上に作成された画像データを、CPUよりビット単位で与えられた矩形の先端値（x_1，y_1）、終端値（x_2，y_2）より、矩形制御部は必要な画像データをメモリアドレス先端値（x_1，y_1）より終端値（x_2，y_2）迄バイト単位にパラメータx_1，x_2の必要なビットを含め、転送時にCPUの介在なしにシステムバスを介してページメモリよりプロッタへのビデオ処理部迄転送する事が可能である。

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【0006】

【実施例】以下、本発明の一実施例を、図面に基づいて詳述する。図1は本発明の画像矩形DMA方式を説明するための全体構成図であり、1はホストコンピュータ、2はCPU、3はROM、4はRAM、5は出図用の文字記号をメモリーしたFONTROM、6はバス制御部、7はページメモリ、8は矩形DMA制御部、9はマスク制御レジスタ、10はビデオ制御部、11はページプリンタであり、図1において、CPU2によってHOST1からROM3，RAAM4，FONTROM5によって出力された画像データがバス制御部6を介してページメモリ7に入力され、1枚分の画像データが完成すると、矩形DMA制御部8にページプリンタ11へ出力する条件が設定され、ビデオ制御部10からのビデオ要求信号に従って矩形DMA制御部8が動作を始め、CPUバスと出力データバスとを切換へるバス制御部6、マスク制御レジスタ9を介してページプリンタ11に必要な画像データ転送される。

【0007】次に、本発明の要旨とする任意の矩形パラメータを与えることによって、ページメモリ7上に作成された画像を、直接ページプリンタ11にDMA出力する方式を、図1に基づき、図2（a），（b），（c），図3および図4を参照しながら説明する。図2（a），（b），（c）はページメモリ7の具体例を示す説明図であり、図（a）においては、CPU2によって出力された1枚分の画像データが示されており、ページメモリ7の先頭値（0，0）、終端値（x_e，y_e）、斜線を施した矩形の先端値（x_1，y_1）、終端値（x_2，y_2）とすると、ページプリンタ11へはこの斜線部分7aのみを転送すればよい。通常は、この斜線部分7aをページプリンタ11に1バイト単位でCPUにより転送されている訳けであるが、本発明ではビット単位でページプリンタ11に転送し、しかもこの転送はCPUによらず、ビデオ制御部10の指令によって矩形DMA制御部8が動作し始め、ページプリンタ11に斜線部分7aが転送される。

【0008】このビット単位で転送する説明は、図（b），（c）に基づいて説明する。図（b）は先端値（x_1，y_1）（以降先端アドレスという）の1バイトに対する無効、有効ビット数を示し、図（c）は終端値（x_2，y_2）（以降終端アドレスという）の1Byteに対する無効、有効ビット数を示す。通常、DMA転送は1バイト，2バイトまたは4バイトであり、1バイトは8ビットであることから、1バイトでの有効，無効ビット数は、無効ビットをαとすると、図2（b）においては、$(x_1/8) = n_1 \cdot (\alpha/8)$、有効ビット数を$\beta$とすると、図2（c）においては、$(x_2/8) = n_2 \cdot (\beta$

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／８）で示される。ここで、n_1 は任意な値における先端アドレス、n_2 は任意な値における終端アドレスを示す。

【０００９】これらのアドレスは、実際上のページメモリ上においては先端アドレスは（x_e ＋１）y_1 ＋ n_1 、終端アドレスは（x_e ＋１）y_2 ＋ n_2 で表される。但し、ｘ方向に関しては$\alpha \neq 0$，$\beta \neq 0$の場合、x_1，x_2のアドレスの有効ビット数は各々（８－α）、βとなる。また、$\beta = 0$の場合、終端アドレスは（x_e ＋１）y_2 ＋ n_2 －１となる。ここで、ＭＡＳＫバイトは１バイト（８ビット）で構成されるデータ０～７ビットの無効ビットを２進法で表現する場合、下位（図１の x_e 方向アドレスを０，１，２……７ビットとした場合の７ビット側から０ビット方向に向った側を示す）３ビットで２進法は総て表現出来ることから、３ビットが必要となる。このように、きめ細かいビット単位で矩形ＤＭＡ制御部８の動作によってページプリンタ11にＤＭＡ転送される訳であるが、次にその動作を、論理回路によって説明する。

【００１０】図３はｘの矩形ＤＭＡ制御部のブロック図であり、矩形の斜線部分7aの先端アドレス（x_1，y_1）、終端アドレス（x_2，y_2）、およびページメモリ７の終端アドレス x_e がセットされると、まずＤＭＡはByte転送の為、各々の割り算器12，16にてByteに変換される。各々のＭＡＳＫ Bit（x_1／８）の下位３ Bit（x_2／８）の下位３ Bitについては、図１で説明した様に、有効ビット数の処理に使用される。但し（x_2／８）の下位３ Bit＝０の場合、減算器18により前述の終端アドレす（x_e ＋１）y_2 ＋ n_2 －１の処理をする為、比較器19には（x_2／８）－１の値がセットされる。そして、ＣＰＵよりこの制御部に起動信号であるＧＯＦ／Ｆがセットされ、ビデオ制御部10より画像同期信号であるＸＣＬＫが入力されてくると、カウンタ14が動き、ｘ方向の有効値を比較器13によりカウンタ値が（x_1／８）より大きいかあるいは等しいかをサーチする。ｘカウンタ14の値が x_e と等しくなると、Ｙカウンタ20を１カウントアップする。Ｙ方向の有効値も比較器21によりカウンタ値がy_1より大きいかあるいは等しいかで有効となる。そして、ｘ方向の終点は比較器19で検出される。同様にY_2 の終点はY_2 比較器22で検出される。

【００１１】以上のようにして、図１の有効値である斜線部分7aが検出される。ページメモリ７に対するアドレスは、ｘカウンタ，Ｙカウンタの値が各々Lower，Upper アドレスになるか、前述の有効範囲のみメモリーリード制御部23でメモリーリード信号が出ない為、ＣＰＵのトータルスループットはこの点でも向上する。図４は図１で示したｘ方向の始点、終点部の有効ビットを決定するブロック図であり、始点の場合下位３ビットは、８ビットに変換する為にｘ，ＭＳＫＳＥＴのタイミングでマスク24に入力され、出力は反転され（有効ビット８－α）、ゲート回路25のゲートを通じてレジスタ30にアイオライト信号（Ｉ／ＯＷ）のタイミングで８ビットのレジスタ30にセットされる。X_1 ＭＳＫＳＥＴが偽の場合（ｘ方向の始点でない場合）、ゲート回路26を通じてレジスタ30にセットされる。ｘ方向の終点の場合、（x_2／８）下位３ビットはX_2 ＭＳＫのタイミングでマスク27を通じて８ビットに変換され、出力はそのままで（有効ビットβ）ゲート回路28を通じてレジスタ30にセットされる。X_2 ＭＳＫＳＥＴが偽の場合（ｘ方向の終点でない）、ゲート回路25を通じてレジスタ30にセットされる。

【００１２】

【発明の効果】以上説明したごとく本発明によれば、ページプリンタ用のページメモリよりＣＰＵの介在なしにページメモリ上に作成されたデータを高速にページプリンタにＤＭＡ転送でき、かつ必要な矩形部分のみのデータをページメモリ上アクセスする為トータルスループットは極めて大となる。又、任意の矩形パラメータのデータの区切りはバイト単位でなくビット単位である為、ハード的にドット単位のクリッピングが可能となる為、トータルスループット及びＣＰＵの負荷が減少できる。

【００１３】

【図面の簡単な説明】

【図１】図１は有効画像データが格納されるページメモリーのイメージ図である。

【図２】図２（ａ），（ｂ），（ｃ）は本実施例の画像矩形ＤＭＡ転送方式の構成を示すブロック図である。

【図３】図３は実施例における矩形ＤＭＡ制御及びページメモリアドレス生成を行なうブロック図である。

【図４】図４は実施例におけるページメモリ上のｘ方向の始点及び終点の有効ビットを決定するブロック図である。

【００１４】

【符号の説明】

1	ホストコンピュータ
2	ＣＰＵ
3	ＲＯＭ
4	ＲＡＭ
5	ＦＯＮＴＲＯＭ
6	バス制御部
7	ページメモリ
8	矩形ＤＭＡ制御部
9	マスク制御レジスタ
10	ビデオ制御部
11	ページプリンタ

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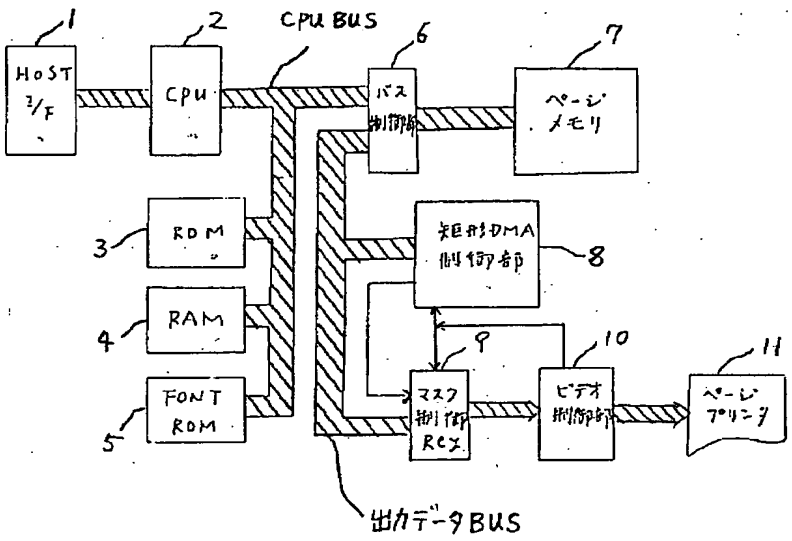
【図1】



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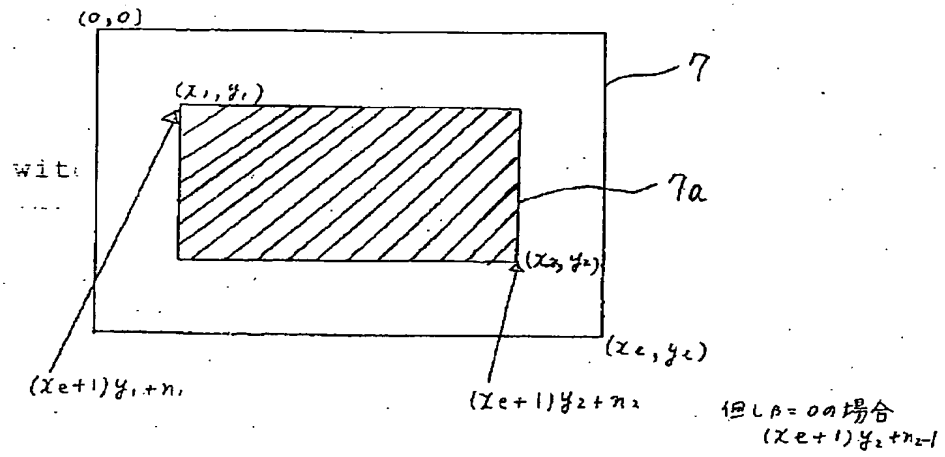
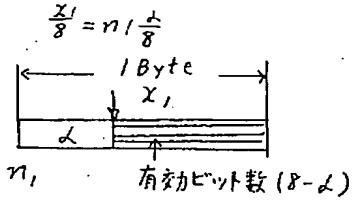
【図2】

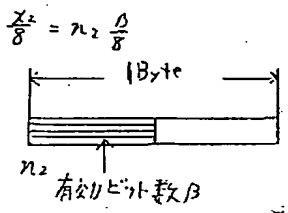
(a)



(b)



(c)



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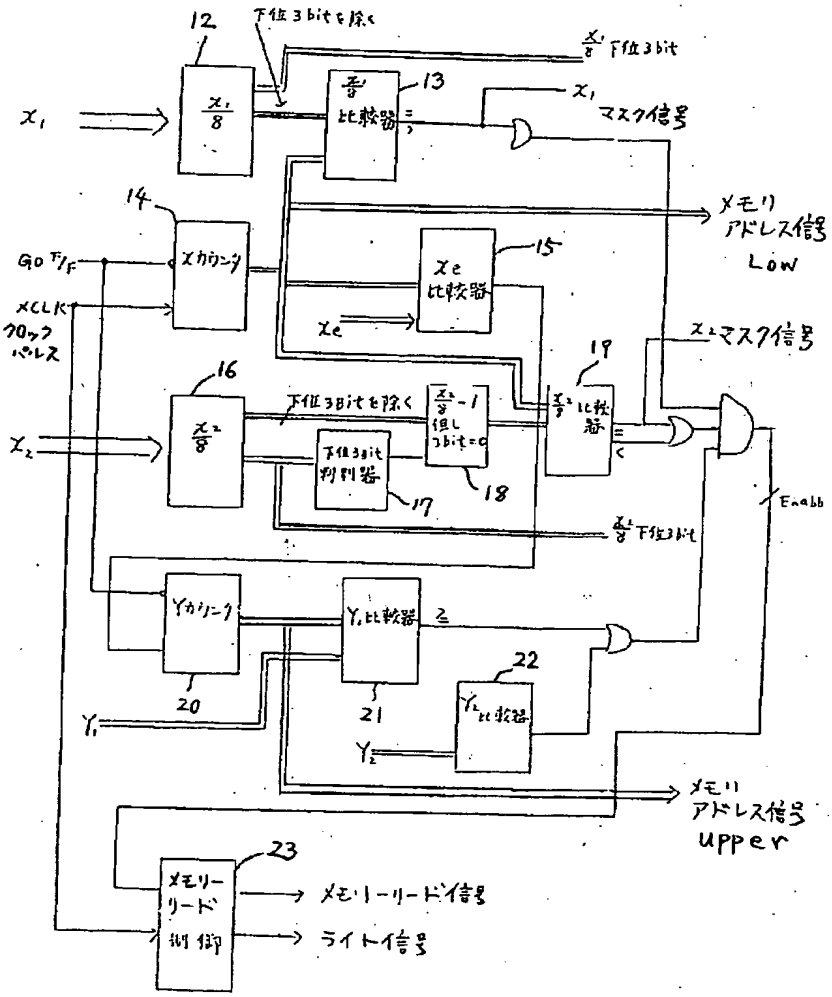
【図３】



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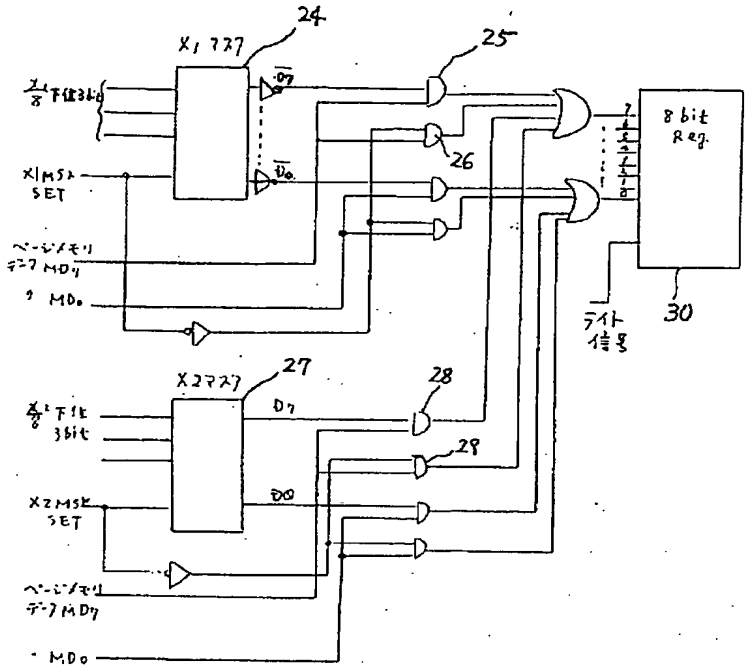
【図4】



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